EE 201 - Digital Hardware Organization - 2 Hours
Required course

1. *2007-2008 Catalog description*
   Continuation of EE101 focusing on the following topics: sequential circuit elements, flip-flops, counters and shift-registers, clock generation circuits, algorithmic state machine method of designing sequential circuits, and VHDL design and synthesis
   Prerequisite: EE101.

2. *Prerequisites by topics*
   a) Boolean algebra, truth tables, DeMorgan's laws
   b) Binary, hex, one's and two's complement number representations; binary arithmetic
   c) Hardware gates: AND, OR, NOT, NAND, NOR, XOR, XNOR
   d) Analysis and design of combinational logic networks: truth tables, circuit minimization via Boolean algebra and Karnaugh maps, and NAND/NOR synthesis
   e) Arithmetic circuits: half and full-adders

3. *Textbook and/or other required materials*
   Required textbook: Electric Fundamentals of Digital Logic, Stephen Brown and Zvonko Vranesic, McGraw Hill Publishing, Second Edition, 2005.
   Required Software: Quartus II (ver. 5 or later) by Altera (http://www.altera.com/)
   (Free download at: www.altera.com/products/software/products/quartus2/qts-index.html)

4. *Class Schedule*
   Two lecture class sessions per week, each 50 minutes, for 14 weeks

5. *Topics Covered (Course Outcomes influenced)*
   a) Design with complex digital logic devices: multiplexers, decoders, encoders, PAL's, CPLD's, and FPGA's. (7a, b, c, d)
   b) Introduction to:
      1. synthesis of combinational logic circuits via VHDL structural, dataflow, and behavioral modeling, and
      2. hardware implementation of combinational logic circuits via Complex Programmable Logic Devices (CPLD's).(7b, c, d)
   c) Sequential logic circuit devices: SR, D, JK, and T flip flops. (7a, b, c, d)
   d) Sequential logic circuit design: state diagrams, present/next state tables, and algorithmic state machine (ASM) flowcharts. (7b, c, d)
   e) MSI sequential logic circuit devices: shift registers and counters. (7b, c, d)
   f) Introduction to:
      1. synthesis of sequential logic circuits via VHDL behavioral modeling, and
      2. hardware implementation of sequential logic circuits via Complex Programmable Logic Devices (CPLD's). (7b, c, d)

6. *Contribution of the course to meeting the professional component*
   Engineering science - 50% , Engineering design - 50%

7. *Course Outcomes (Program Outcome contributions): To ensure students attain the following outcomes, graded deliverables are used to measure performance relative to the outcomes.*
   a) Students will design basic digital logic subsystems. (9A, B, C, D)
   b) Students will analyze and design basic synchronous sequential logic circuits. (9A, B, C, D)
   c) Students will use a hardware description language and an appropriate professional level computer-aided design (CAD) package for digital logic design, simulation, and implementation. (9B, C, D)
   d) Students will implement a relatively complex finite state machine design project in a Complex Programmable Logic Device utilizing the hardware description language and CAD package referenced in 7c above. (9A, B, C, D, G)

8. *Grading Policy*
The degree to which students achieve the course outcomes is determined by the following grading policy.

Grades will be dictated by the results of three one-hour exams and two demonstrated VHDL design projects based on the following percentages.
Exam 1: 100 points (25%)
Exam 2: 100 points (25%)
Exam 3: 100 points (25%)
Project 1: 30 points (7.5%)
Project 2: 70 points (17.5%)

The two VHDL design projects are to be completed independently by each student. Therefore, students are expected to design and implement their projects with assistance obtained exclusively from the instructor, and collaboration between students will be considered a form of cheating. Letter grades will be assigned for each exam to provide students with a grade estimate throughout the semester, but the final course grade will be determined by a curve based on the combined numerical results of all three exams and the two VHDL design projects. Although the arithmetic mean of the combined numerical results will usually correspond to a "middle" B, the letter grade corresponding to the arithmetic mean may be shifted up or down based on the performance of the present class with respect to the degree to which students meet the course outcomes specified in item 7 above. A grade of 'C' corresponds to minimum acceptable level of competency relative to the course outcomes. Exams missed without prior approval will result in a zero for that exam. In addition, cheating on examinations or projects will be dealt with as described in the Bradley University Academic Handbook.

8. *Relationship of course to program outcomes*

label	Program Outcomes (A Graduate from the program will:)	Contribution
A	have knowledge of the mathematical and scientific foundation of electrical engineering	Strong
B	have knowledge of and the ability to apply techniques and technology of electrical engineering	Strong
C	complete a design project sequence, culminating in a capstone project at or near the professional level	Moderate
D	understand that acquisition of new knowledge is needed for success in the electrical engineering profession	Moderate
E	meet Bradley's general education requirements which are based on the principles of liberal education	NA
F	have experience in communicating technical information and working on teams	Foundational
G	understand the importance of professional and ethical behavior	Moderate

10. *Prepared by:*
Steven D. Gutschlag: Date: 11/15/07